Remarks:

Reconsideration of the application is requested.

Claims 15-30 remain in the application.

In item 5 on page 3 of the above-identified Office action, the drawings have been objected to as failing to comply with 37 CFR 1.84(p)(4).

More specifically, the Examiner has stated that reference character 30 has been used to designate both compensation zones and pillars. Reference character 30 has been used to designate only one element in the figures. Perhaps the language on page 8, lines 23-30 of the translated specification could have been expressed more clearly. If the Examiner will once again refer to that language, it is believed that the Examiner will see that the term "pillars 30" refers to the pillar shaped compensation zones. The language has been changed to more clearly reflect this. Support for the changes can be found by referring to page 8, line 23 through page 9, line 2 and to fig. 1.

In item 6 on page 3 of the above-identified Office action, the drawings have been objected to as failing to comply with 37 CFR 1.84(p)(5).

Compensation zones 30E are described at page 15, line 12.

P-doped layer 32 is described at page 9, lines 6-9 and at page 13, line 20.

Reference characters 27 and 31 have been deleted from Fig. 6. The indication of the error is appreciated.

In item 9 on page 3 of the Office action, claims 15-21, 24, 27, and 30 have been rejected under 35 U.S.C. § 101 as claiming the same invention as claims 1-12 of Tihanyi (U.S. application No 10/033,122). Applicants respectfully traverse.

The same invention is not being claimed. Same invention means identical subject matter. Claim 15 of the instant application defines a semiconductor component with three layers, namely a substrate of a first conduction type, a first layer of a second conduction type (n), and a second layer of the second conduction type configured between the substrate and the compensation zones formed in the first layer.

In contrast, claim 1 of U.S. application No 10/033,122 defines a semiconductor component with only two layers, namely a first layer of a first conduction type, and a second layer of the first conduction type lying above said first layer. Identical subject mater is not being claimed. Please see MPEP 804 II(A).

In item 11 on page 6 of the Office action, claims 22, 23, 25, 26, 28, and 29 have been rejected under 35 U.S.C. § 101 as claiming the same invention as claims 1-12 of Tihanyi (U.S. application No 10/033,122). Applicants respectfully traverse.

Tihanyi (U.S. application No 10/033,122) does not teach or suggest the invention defined by claim 15 in the present application. Claim 15 of the instant application defines a semiconductor component with three layers, namely a substrate of a first conduction type, a first layer of a second conduction type (n), and a second layer of the second conduction type configured between the substrate and the compensation zones formed in the first layer. The three layer configuration is not an obvious variation of the previously claimed two layer configuration, and it is respectfully submitted that the Examiner has not given any support for such an allegation, and in fact has not made such an allegation.

In item 13 on page 6 of the Office action, claims 15-30 have been rejected as being anticipated by German Patent Application 100 52 170.3 under 35 U.S.C. § 102. Applicants respectfully traverse.

The Examiner has cited applications own application from which priority has been claimed. The rejection is improper.

Counsel's file indicates that a claim for priority was made and a certified copy of German Patent Application 100 52 170.3 had been filed on December 20, 2001.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 15, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 15-30 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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January 7, 2003

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WMP-SME-515·

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jenoe Tihanyi

Applic. No. : 10/007,397

Filed : October 22, 2001

Title : Semiconductor Component

Examiner : Monica Lewis

Group Art Unit : 2822

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Translated Specification:

On page 8, lines 23-30:

P[p]-doped compensation zones 30 are formed in the n-doped layer 24 and, in the exemplary embodiment according to figure 1, extend in a pillar-shaped manner in the vertical direction of the semiconductor body 20. The cross section of these [pillars] pillar shaped compensation zones 30 is circular in the exemplary embodiments according to figures 2 and 3, but this cross section can assume virtually any other geometric shapes and be, for example, rectangular, square or octagonal.